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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,069	07/23/1999	PETER WOHL	SNSY-A1998-0	3639

35273 7590 11/30/2004

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EXAMINER	
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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 November 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *37-53 and 55-58*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☒ Other: *See attachment.*

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

ADVISORY ACTION

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named inventor is: WOHL
3. Applicant's After Final Amendment was received 11/2/04.
4. Thus, claims 37-53 and 55-58 are pending. The independent claims are: 37, 51, 53, and 55.
5. The US filing date is 7/23/99, and no earlier priority is claimed.

Index of Prior Art and Dictionaries

6. Cheng refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.
7. Beausang'771 refers to US Patent 5,696,771.
8. "Using Verilog Simulation Libraries for ATPG" refers to "Using Verilog Simulation Libraries for ATPG", 0-7803-5753-1/99 1999 IEEE, by Peter Wohl, and John Waicukauski (Publication date 28-30 Sept. 1999).
9. "Testing "untestable" faults in three-state circuits" refers to "Testing "untestable" faults in three-state circuits" by Wohl et al, 0-8-86-7304-4/96, 1996, IEEE pages 324-333.
10. Tucker refers to "The Computer Science and Engineering Handbook", by Allen B. Tucker, CRC Press, ISBN: 0-8493-2909-4, 1996, pages 450-453.
11. Smith refers to "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 38-40.
12. MS Dictionary refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
13. McGraw-Hill Dictionary refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., 2003, ISBN 0-07-042313-X.
14. IEEE Dictionary refers to The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

Definitions

15. **"Associative memory"** is defined as "A type of memory whose locations are identified by their contents or by a part of their contents, rather than by their names or positions. Synonyms: search memory, content addressable storage" by IEEE Dictionary. Note that Tucker page 450-453 states "The cache memory is associative, or content-addressable. In an associative memory, the address of a memory location is stored, along with its content. Rather than reading data directly from a memory location, the cache is given an address and responds by providing data which may or may not be the data requested. When a cache miss occurs, the memory access is then performed with respect to the backing storage, and the cache is updated to include the new data."
16. **"Automatic test pattern generator (ATPG)"** as "Any tool that generates test information for a device based on structural analysis of the device", by IEEE Dictionary.
17. "**Content addressable memory**" (CAM) is defined as "See: associative memory" by IEEE Dictionary.
18. "**Logical**" is defined as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values... Boolean algebra", by MS Dictionary.
19. **"Primitive"** is defined as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program", by McGraw-Hill Dictionary.
20. **"Primitive"** is defined as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants", by MS Dictionary.
21. "**Random access memory**" (RAM) is defined as "(1) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location (adapted from IEC 748-2). Note: The term RAM, as commonly used, denotes a read/write memory with unlimited data rewrite capability and equal read and write times." by IEEE Dictionary.

Applicant's Remarks received 11/2/04

22. Remarks page 2. Applicant accurately states that only Beausang'771 is used for the rejection of claims 37-47, 49, 51-53, and 55-58, and Applicant requests clarification. Applicant is correct that the rejection should more clearly state that claims 37-47, 49, 51-

53, and 55-58 are rejected only under 35 USC 102(b) as anticipated by Beausang'771. The rejections have been rewritten to be more clear with respect to these claims. Only claims 48 and 50 are rejected under 35 USC 103 with over Beausang'771 in view of "Testing" by Wohl. These clarified rejections are presented below.

23. Remarks page 2. Applicant asserts that the combination of Beausang and Testing is "inappropriate". Applicant does not address the specific motivation stated by the rejection, and thus is not persuasive. The motivation from the rejection is repeated here for convenience: "At the time of the invention, one of ordinary skill in the art would have been motivated to use "Testing "untestable" faults in three-state circuits" by Wohl et al to modify Beausang'771 in order to "increased test coverage... while decreasing CPU time" according to the Abstract of "Testing "untestable" faults in three-state circuits" by Wohl et al."
24. Remarks page 3-22. Applicant asserts that the specific limitations of all pending claims are not disclosed by Beausang or "Testing", as mapped in the rejection. However, one of ordinary skill in the art would interpret Beausang and Testing as disclosing all of the claim limitations, in view of the definitions of "primitive" from McGraw-Hill Dictionary and from MS Dictionary, and in view of Beausang's discussion of primitives at column 1 lines 42-67.
25. Specifically, for example, at Remarks page 5 Applicant asserts that "the primitives of Beausang are used to model logic, and not memory as recited by the Applicants". Emphasis in original. **This assertion is not persuasive because Beausang explicitly considers memory to be a "primitive" cell. Beausang column 1 line 53 states "netlist can include primitive cells such as... latches and D-flip flops etc."** Note that latches and D-flip flops are specific types of memory.
26. Further, even if Beausang did not explicitly disclose "latches and D-flip flops", these (relatively complex memory) primitive cells are created by small groups of (relatively less complex) primitive cells. In other words, memory is formed by combinations of smaller logical elements.
27. Similarly, the Beausang column 1 lines 42-67 term "netlist... primitive cells... and their interconnections" discloses Applicant's claim term "port".

28. Thus, Applicant's assertions are not persuasive, and the rejections are maintained.

Claim Rejections - 35 USC § 102(b)

29. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
30. Claims 37-47, 49, 51-53, and 55-58 are rejected under 35 USC 102(b) as being anticipated by Beausang'771.
31. Independent claim 37 is a "memory model" claim with 5 limitations, numbered by the Examiner for clarity.
32. [1]-**"a memory primitive** comprising a write address port, a write data port, and an output port"
33. [2]-**"a read data port primitive** comprising a read data port for coupling to the output port of the memory primitive, a read address port, and an output port"
34. [3]-**"an address bus primitive** comprising an output port for coupling to the write address port of the memory primitive and the read address port of the read data port primitive"
35. [4]-**"a data bus primitive comprising an output port** for coupling to the write data port of the memory primitive"
36. [5]-**"a plurality of memory out primitives,** each memory out primitive comprising an input port for coupling to the output port of the read data port primitive"
37. The above 5 limitations are disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION". Note that the column 1 line 55 term "latches and D-flip flops" disclose

memory primitives. Further note that column line 56 "and their interconnections" discloses address bus and data bus.

38. In claim 38, there are 4 limitations:
39. [1] **"a set input port"**
40. [2] **"a reset port"**
41. [3] **"a write_clock port"**
42. [4] **"a write_enable port"**
43. The above 4 limitations are disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
44. In claim 39, **"the read data port primitive represents a read port functionality of the memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
45. In claim 40, **"wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then

applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

46. In claim 41, **"the address bus primitive represents an address functionality of a memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
47. In claim 42, **"the address bus primitive includes: a plurality of input ports corresponding to an address dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
48. In claim 43, "**the address bus primitive** further includes an attribute indicating whether an incoming address is encoded or decoded" is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist",

and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

49. In claim 44, **"the data bus primitive represents a data bus functionality of the memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
50. In claim 45, **"a plurality of input ports corresponding to a data dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
51. In claim 46, **"each memory out primitive represents a simulated value storage functionality of the memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9

element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

52. In claim 47, **"an output port"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
53. In claim 49, "a plurality of edge-triggered registers can be coupled to the output ports of the memory primitives, thereby representing an attribute of the read data port primitive" is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
54. Claim 51 is an independent "content addressable memory model" claim with 5 limitations:
55. [1]-**"a memory primitive including an output port"**
56. [2]-**"a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port"**
57. [3]-**"a data bus primitive for coupling to the memory primitive"**
58. [4]-**"a plurality of memory out primitives, each memory out primitive for coupling to the compare port primitive"**

59. [5]-**"an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives"**
60. The above 5 limitations are disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
61. In claim 52, "a compare enable port for receiving a compare signal" is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
62. Claim 53 is an independent "combined CAM and RAM model" with 11 limitations:
63. [1]-**"a first memory primitive including an output port"**
64. [2]-**"a data bus primitive including an output port"**
65. [3]-**"a compare port primitive... comprising ; a compare enable port"**
66. [4]-**"a data bus port for coupling to the output port of the first memory primitive"**
67. [5]-**"a data port for coupling to the output port of the first memory primitive"**
68. [6]-**"a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive"**

69. [7]-**"an address bus primitive including an output port and an input port for coupling to the output port of the compare port primitive"**
70. [8]-**"an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives"**
71. [9]-**"a second memory primitive including an output port"**
72. [10]-**"a read data primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives"**
73. [11]-**"a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive"**
74. The above 11 limitations are disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
75. Claim 54 has been cancelled.
76. In claim 55, **"a plurality of primitives, each primitive representing a defined functionality of a memory"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9

element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

77. In claim 56, **"each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool"** disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
78. In claim 57, **"the behavioral HDL includes Verilog"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION". Note that Verilog is one of the two most common HDL languages: Verilog and VHDL.
79. In claim 58, **"the subset of behavioral HDL can directly map to the plurality of primitives"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790

"VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION". Note that Verilog is one of the two most common HDL languages: Verilog and VHDL.

Claim Rejections - 35 USC § 103

80. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
81. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.
82. **Claims 48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of "Testing "untestable" faults in three-state circuits".**
83. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of "Testing "untestable" faults in three-state circuits".
84. Claim 48 depends from claim 47, with one additional limitation which is not disclosed by Beausang'771.
85. In claim 48, the additional limitation **"a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive"** is disclosed by "Testing "untestable" faults in three-state circuits" by Wohl et al, at Abstract "tristate... test generation techniques".
86. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of "Testing "untestable" faults in three-state circuits".
87. Claim 50 depends from claim 49, with one additional limitation which is not disclosed by Beausang'771.
88. In claim 50, the additional limitation **"input ports of a plurality of tristate drivers can be coupled to the output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive"** is disclosed by "Testing

"untestable" faults in three-state circuits" by Wohl et al, at Abstract "tristate... test generation techniques".

89. **MOTIVATION.** At the time of the invention, one of ordinary skill in the art would have been motivated to use "Testing "untestable" faults in three-state circuits" by Wohl et al to modify Beausang'771 in order to "increased test coverage... while decreasing CPU time" according to the Abstract of "Testing "untestable" faults in three-state circuits" by Wohl et al.

Conclusion

90. All pending claims stand rejected.

Communication

91. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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